



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Inventors: Takaharu SAEKI, et al.

Application No.: 10/581,262

Filed: June 1, 2006

For: DELTA-SIGMA TYPE FRACTION DIVISION PLL
SYNTHESIZER

INFORMATION DISCLOSURE STATEMENT

Assistant Commissioner of Patents
Washington, DC 20231

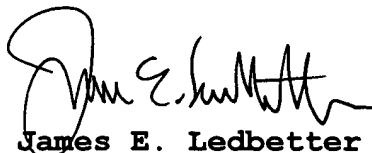
Dear Sir:

Pursuant to Rules 56 and 99, Applicants hereby call the attention of the Patent Office to the documents listed on the attached Form PTO 1449. WO '604 corresponds to JP '894. JP '044, JP '894, the Adachi, et al. reference and the Matsuya, et al. reference are cited on page 5 of the Specification. The Hegazi, et al. reference is cited on page 6 of the Specification.

Applicants present this art so that the Patent Office may, in the first instance, determine any relevancy thereof to the presently claimed invention, see Beckman Instruments, Inc. v. Chemtronics, Inc., 439 F.2d 1369, 1380, 165 USPQ 355, 364 (5th Cir. 1970). Also see Patent Office Rules 104 and 106. Applicants respectfully request that this art be expressly considered during the prosecution of this application and made of record herein and

appear among the "References Cited" on any patent to issue herefrom.

Respectfully submitted,



James E. Ledbetter
Registration No. 28,732

Date: August 29, 2006

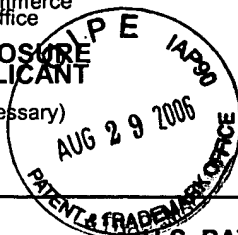
JEL/jpf

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FORM PTO-1449 U.S. Department of Commerce
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use several sheets if necessary)



ATTY. DOCKET NO.

L8462.06108

SERIAL NO.

10/581,262

APPLICANT

T. SAEKI, et al.

FILING DATE

June 1, 2006

GROUP

Unassigned

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE

FOREIGN PATENT DOCUMENTS

	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
						YES	NO
	2002 1 5 2 0 4 4	05/2004	JP			X	
	5 5 0 0 8 9 4	02/1993	JP				
	9 1 1 7 6 0 4	11/1991	WO				

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

H. Adachi, et al.: "High-Speed Switching Synthesizer Using Fractional N Phase Locked Loop," The Institute of Electronics, Information and Communication Engineers, Transactions C-1, Vol. J76-C-1, No. 11, November 1993, pages 445-452, with partial English translation.

Y. Matsuya, et al.: "A 17-njt Oversampling D-to-A Conversion Technology Using Multistage Noise Shaping," IEEE Journal of Solid-State Circuits, vol. 24, No. 4, August 1989, pages 969-975.

E. Hegazi, et al.: "A 17-mW Transmitter and Frequency Synthesizer for 900-MHz GSM Fully Integrated in 0.35-μm CMOS," IEEE Journal of Solid-State Circuits, Vol. 38, No. 5, May 2003, pages 782-792.

EXAMINER

DATE CONSIDERED

EXAMINER: Initial if citation is considered, draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.